AGENDA

• Progress
  • 14nm Update
  • Cost per Transistor Trend

• Economics of Moore’s Law
  – What does it take to afford to continue?

• Competitiveness

• Forward looking options
14 NM PRODUCT YIELD IS IN HEALTHY RANGE

22nm Is Intel’s Highest Yielding Process Ever
Increasing Yield

14 nm Yield Is Maturing

22 nm data are shifted to align date of lead product qual

Trending to match 22nm yields

Source: Intel
COST PER TRANSISTOR TREND

Source: Intel estimate, based upon available information and subject to change
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Moore’s Law Enables Innovation and Cost Reductions

- Twice the circuitry in the same space (architectural innovation)
- Same circuitry half the space (cost reduction)

Option to design for optimal performance/cost

Source: Intel
ADVANCING PROCESS TECHNOLOGY LOWERS COSTS

Ten Year Model of Manufacturing and Process R & D

2011 Analysis

$302B

Same process for ten years

$104B

Develop new processes

Process R & D

Manufacturing Costs

Assumptions are theoretical and not forecasts.

Source: Intel
ADVANCING PROCESS TECHNOLOGY LOWERS COSTS

Ten Year Model of Manufacturing and Process R & D

2015 Update

$116B

Develop new processes

$270B

Same process for ten years

Assumptions are theoretical and not forecasts.
Source: Intel
THREE WAYS TO TEST THE MODEL:

- Lower unit demand
- Higher technology development cost
- Reduced cost per transistor improvement
Three Ways To Test The Model: Unit Demand Changes

Annual unit demand of -25% over 10 years required to offset economic scaling benefits

Assumptions are theoretical and not forecasts
Source: Intel
THREE WAYS TO TEST THE MODEL: R&D COST INCREASES

By Year 10, R&D Would Be > $80B / Year

Higher R&D investment growth will NOT limit Moore’s Law

Assumptions are theoretical and not forecasts.

Source: Intel
THREE WAYS TO TEST THE MODEL: \textbf{CPT IMPROVEMENT REDUCES}

Poorer CPT scaling could challenge economic benefits

Assumptions are theoretical and not forecasts
Source: Intel
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LOGIC AREA SCALING TREND
(Publicly available scaling information)

Source: Intel data from shipping products
Otherwise based on published information.
70nm: E. Jantsch (IBM storage, 2000 ISM, p. 63)
90nm: H. Shin (IBM reliability, 2000 ISM, p. 129)
120nm: T. Win (IBM 1995-1999, p. 22)
ESTIMATED FULL CHIP SCALING

Area scaling estimate includes more of the technology features

Updated from Investor Meeting 2013

Full Chip Area

- Intel
- TSMC
- Samsung

Log Scale

32/28 nm  22/20 nm  14/16 FinFET* nm  10 nm*


Other names and brands may be claimed as the property of others.
TRANSISTOR DENSITY FROM ACTUAL PRODUCTS

Source: Intel Internal analysis
Other names and brands may be claimed as the property of others.
**COMPOSITION MATTERS**

SRAM density = ~ 3X+ of logic
Logic cell choice = ~ 3X

A8/A9 has more inherently dense elements. Intel has more sparse, higher speed elements.
TRANSISTOR DENSITY NORMALIZED FOR COMPOSITION

Product data demonstrates Intel 14nm advantage

Source: Intel internal analysis

Other names and brands may be claimed as the property of others.
Intel 14nm provides significant density advantage


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Future Options Being Investigated

FUNCTION

Quantum Computing

Flexible/Stretchable

Sensors/Actuators

HETEROGENEOUS INTEGRATION

SELECTIVE DEPOSITION

DIRECTED SELF-ASSEMBLY

SCALING

High Voltage RF, mm-Wave

GaN Transistors

RRAM and STTM

Nanowire

Tunnel FET

III-V

III-V

Spin-based

Source: Intel
SUMMARY

• 14nm yields, availability and product portfolio **MATURING**
• Cost per Transistor is difficult, but progress is **PROMISING**
• Economics of Moore’s Law for Intel are **SOLID**
• Our view of competition is **UNCHANGED**
• Innovation and change will be required looking forward but....
• The research pipeline is challenging but **FULL**
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